APM32F103xB

Errata Sheet

Version: V 2.0

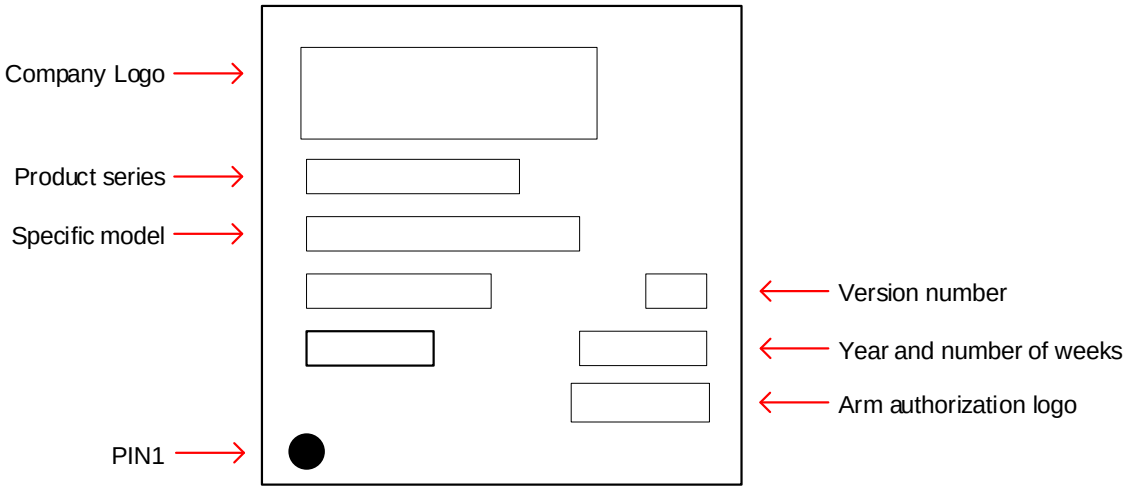
Contents

1 Introduction

This manual mainly introduces the limitations of the APM32F103xB series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Product Version and Silk Screen Printing Instructions

Figure 1 Product Version and Silk Screen Printing Instructions



3 Errata List

Table 1 Errata List

Category	Introduction	Product version		
		B3	D1	E1
GPIO	GPIO output	●	●	●
	PA12 cannot directly output the EVENTOUT signal of Arm® Cortex®-M3 core	●	●	×
	SPI1 and I2C1 remapping	×	×	●
	PC8 output exception pulse	?	?	?
System	PWR sleep mode	●	●	●
	Float variable exception	●	●	●
ADC	Calibration exception	●	●	×
Flash	The read-only area can be modified by applications	●	●	●
	Wait cycle	●	●	×
Clock	HSE serves as the clock source	●	●	●
	LSE startup	●	●	×
	PLL frequency multiplication	●	●	×
	After Standby in low-power mode is awakened, the HSI frequency is below 8Mhz	×	×	●
	At high temperature, some chip LSE vibrates abnormally or stops vibration	●	●	×
USART	USART hardware flow control	×	×	●
SPI	Module timing of SPI	●	●	×
USBD/CAN	USBD interrupt	×	×	●
	Combined use of USBD/CAN	×	×	●
	CAN communication	●	●	●
Tool	Burning	●	●	●
	Zhengdian Yuanzi offline download	●	●	●

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

4 GPIO

4.1 GPIO output

Problem description

When the GPIO port is configured as multiplexing push-pull output, the output voltage may be affected by external interference and is unable to output accurate levels; when configured as floating input to read the external I/O input values, it may be affected by external interference and is unable to read accurate values.

Solutions

When configured as multiplexing push-pull output, connect an external pull-up resistor; when configured as floating input, connect an internal pull-up resistor externally or configure it as a pull-up input.

4.2 PA12 cannot directly output the EVENTOUT signal of Arm® Cortex®-M3 core

Problem description

PA12 cannot directly output the EVENTOUT pulse signal of Arm® Cortex®-M3 core.

Solutions

Choose either of the following solutions:

- When PA12 outputs EVENTOUT pulse signal of Arm® Cortex®-M3 core, CAN_TX must be remapped first.
- Related problems can be solved by migrating the E1 version.

4.3 SPI1 and I2C1 remapping

Problem description

After PB5 pin is remapped to SPI1 function and I2C1 clock is enabled, SPI cannot communicate normally due to the conflict between SPI1 MOSI and I2C1 SMBA signals.

Solutions

Do not use the remapping and I2C1 functions in SPI1 master mode simultaneously. When SPI1 is remapped, the clock of I2C1 must be turned off.

4.4 PC8 output exception pulse

Problem description

When some F103XB D1 version chips are powered on, PC8 emits a 1us abnormal pulse.

Solutions

Choose either of the following solutions:

- Do not use PC8 to drive sensitive circuits, or filter out this pulse with a small capacitor at the PC8 output port.
- Related problems can be solved by migrating the E1 version.

5 System

5.1 PWR sleep mode

Problem description

The PWR sleep mode_WEF() instruction is invalid and cannot enter the low-power mode.

Solutions

Choose either of the following solutions:

- Execute normally after the pin is reset.
- Set in the download interface of Keil (set the reset and run).
- Add the second WFE instruction and it can be executed normally.
- Use 1 WFI rather than WFE.

5.2 Float variable exception

Problem description

Use the compilation project to add sc_math.lib to the engineering, and the program will crash when using a float variable.

Solutions

As long as sc_math.lib is added, the FPU clock must be enabled.

6 ADC

6.1 Calibration exception

Problem description

After the frequency of ADC_PCLK2 is divided by eight, it is used as an ADC clock, but a calibration exception occurs when configuring ADC1/2 repeatedly.

The specific situation is: After the frequency of PCLK2 is divided by eight, it is used as an ADC clock, but calibration can be finished when configuring ADC1/2 for the first time. Do not enable ADC1/2, and then configure ADC1/2, or a calibration exception will occur, and the reset calibration RSTCAL cannot be cleared to zero.

Solutions

Choose either of the following solutions:

- Enable ADC before configuring it.
- Related problems can be solved by migrating the E1 version.

7 Flash

7.1 The read-only area can be modified by applications

Problem description

The value of read-only area address 0x1FFFF7D0 can be modified by the application.

Solutions

When executing the codes, the wait cycle of Flash is modified for different clock frequencies due to the read speed of Flash.

7.2 Wait cycle

Problem description

When switching the system clock in RCC (such as switching HSE-PLL9 multiplication), and the wait cycle of Flash is set to 1 at 72MHz, the program is abnormal.

Solutions

Choose either of the following solutions:

- Configure the Flash wait cycle strictly according to the Manual, and ensure that the value of the Flash wait cycle matches the system clock. The relationship between the APM32 system frequency and the Flash wait cycle is:

  0 wait cycle, when 0<SYSCLK<24MHz

  1 wait cycle, when 24<SYSCLK<48MHz

  2 wait cycles, when 48<SYSCLK<72MHz

  3 wait cycles, when 72<SYSCLK<96MHz

- Related problems can be solved by migrating the E1 version.

8 Clock

8.1 HSE serves as the clock source

Problem description

When the timeout value of the software that sets the HSE startup time is too small (e.g. 0x0500), external clock startup ready timeout may occur, which may result in the failure of using HSE as the clock source.

Solutions

To ensure normal startup of the crystal oscillator, it is recommended to modify the external clock wait time timeout value to at least 0x3200.

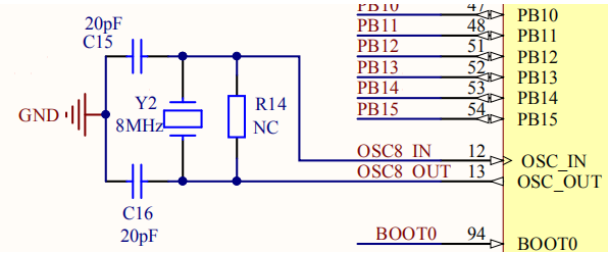
The specific operation is modifying the macro definition of HSE_STARTUP_TIMEOUT. Macro definition varies depending on the version of the library function:

- For the V3.x version library functions, the macro definition is in XXX32F10x.h;
- For the library before V3.0, the macro definition is in XXX32f10x_RCC.c.

The recommended crystal oscillator circuit is shown below (the capacitance value should match the crystal oscillator model)：

#define HSE_STARTUP_TIMEOUT ((uint16_t)0x3200) (recommended 0x3200, maximum 0xffff).

Figure 2 Crystal Oscillator Circuit



8.2 LSE startup

Problem description

When the system is powered on for the first time, and the external low-speed clock enable ready flag is set, the external low-speed clock may still be beyond the standard frequency range and it takes a certain delay time to achieve stable clock output.

Solutions

Choose either of the following solutions:

- It is recommended that when the external low-speed clock enable ready flag is set, a delay of about 100ms should be inserted in the software to wait for the clock frequency to be stable, or wait for about 2s before using the LSE.
- Related problems can be solved by migrating the E1 version.

8.3 PLL frequency multiplication

Problem description

After doubling to 24MHz using PLL, the frequency output through the PA8 pin is unstable.

Solutions

Choose either of the following solutions:

- When using PLL multiplication, first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.
- Related problems can be solved by migrating the E1 version.

8.4 After Standby in low-power mode is awakened, the HSI frequency is below 8Mhz

Problem description

After the Standby of the chip in low-power mode is awakened, the HSI frequency is below 8Mhz

Solutions

Choose either of the following solutions:

- Solve related problems by migrating the D1 version.
- After Standby is awakened, perform a software reset, and after MCU restarts, restore the HSI to 8MHz;
- Change to use HSE as the clock source;

8.5 At high temperature, some chip LSE vibrates abnormally or stops vibration

Problem description

When the chip is at high temperature, the LSE may vibrate abnormally or stop vibrating.

Solutions

Choose either of the following solutions:

- Related problems can be solved by migrating the E1 version.
- Geehy can be requested to provide chips that have undergone high-temperature screening.

9 USART

9.1 USART hardware flow control

Problem description

USART1 is configured as hardware flow mode, CAN_TX is not remapped, and USART1_RTS cannot be used normally.

Solutions

Remap CAN_TX and USART1_RTS can be used normally.

10 SPI

10.1 Module timing of SPI

Problem description

When SPI (SPI_cmd() function ENABLE) is enabled, after SPI parameters are modified, the timing transmission of SPI for one byte is 16 clocks (normally 8 clocks).

Solutions

Choose either of the following solutions:

- The initialization standard operation of SPI is specifically: Initialize the corresponding SCK, MOSI, MISO and NSS, and enable SPI. To modify the parameters, first enable SPI (SPI_cmd() function DISABLE) and then modify the corresponding configuration.
- Related problems can be solved by migrating the E1 version.

11 USBD/CAN

11.1 USBD interrupt

Problem description

If the DM and DP data cables of USBD are both at high level, an abnormal interrupt will be caused and the operation of the main program will be affected. This is an unconventional operation.

Solutions

Choose either of the following solutions:

- Add the code suspended by FSUSP by force to the ESOF flag judgment of the USBD interrupt function.
- When starting the chip, first determine whether the I/O of D- is at a high or low level.
  - If it is at a high level, it indicates that it has been inserted into a charging device, and USBD initialization will be skipped, without enabling the USBD function;
  - If it is at a low level, it indicates that it has been inserted into a normal host, USBD is initialized normally, and USBD function is enabled.

11.2 Combined use of USBD/CAN

Problem description

USBD1 and CAN2 of APM32F103xB_E can be used simultaneously, USBD2 and CAN1 can be used simultaneously, USBD1 and USBD2 cannot be used simultaneously, and CAN1 and CAN2 can be used simultaneously.

Solutions

Use according to the recommendations of *Datasheet* and *User Manual*.

11.3 CAN communication

Problem description

When HSI is used as a clock source, CAN communication may fail.

Solutions

It is recommended to use HSE as the clock source when using the CAN function.

12 Tool

12.1 Burning

Problem description

When the xT packet is used on Keil5.27 version, it cannot be burnt through AP-LINK and ULINK2.

Solutions

Choose either of the following solutions:

- Use APEXMIC.APM32F1xx_DPF or keil.xTM32F1xx.DFP.2.2.0.pack.
- Modify keil.xTM32F1xx.DFP.pdsc, and the specific operation is as follows:

(1) Look for keil.xTM32F1xx.DFP.pdsc under the installation directory of Keil;

(2) Select the file, and right-click to choose the attributes;

(3) Remove the read-only attribute of the file;

(4) Open keil.xTM32F1xx.DFP.2.2.0.pack, to find the location of Not a genuine xT Device! Abort connection;

(5) Try to find the following content:

<!--

Query(0,” Not a genuine xT Device! Abort connection” ,1);

Message(2,” Not a genuine xT Device! Abort connection.”);

-->

(6) Log out.

13 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	1.0	New edition

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